AMENDMENT TO THE CLAIMS

Please **ADD** claims 49-56 as follows:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-30 (Canceled).

Claim 31. (Previously Presented) A method of fabricating a semiconductor structure, comprising the steps of:

forming a $Si_{1-x}Ge_x$ layer on a multi-layer substrate;

forming a plurality of channels in the $Si_{1-x}Ge_x$ layer and in a top layer of the multi-layer substrate;

after forming the plurality of channels, removing the top layer of the multi-layer substrate underneath the $Si_{1-x}Ge_x$ layer to form a void defined by an undercut border in the multi-layer substrate; and

filling the channels and the void with a dielectric material.

Claim 32. (Previously Presented) The method of claim 31, wherein the dielectric material comprises silicon dioxide.

Claim 33. (Previously Presented) The method of claim 31, further comprising, after the forming of the $Si_{1-x}Ge_x$ layer, forming a cap layer on the $Si_{1-x}Ge_x$ layer.

Claim 34. (Previously Presented) The method of claim 33, wherein the forming of a plurality of channels comprises forming a plurality of channels in the cap layer, the

$Si_{1-x}Ge_x$ layer, and the top layer of the multi-layer substrate.

Claim 35. (Previously Presented) The method of claim 31, further comprising removing the cap layer after the filling of the channels and the void with the dielectric material.

Claim 36. (Previously Presented) The method of claim 31, further comprising removing a cap layer arranged above the $Si_{1-x}Ge_x$ layer after the filling of the channels and the void with the dielectric material.

Claim 37. (Previously Presented) The method of claim 36, further comprising forming a strained Si layer on the $Si_{1-x}Ge_x$ layer.

Claim 38. (Previously Presented) The method of claim 36, wherein the forming of the strained Si layer is a step that includes one of:

ultrahigh vacuum chemical vapor deposition (UHVCVD);
rapid thermal chemical vapor deposition (RTCVD);
low-pressure chemical vapor deposition (LPCVD)
limited reaction processing CVD (LRPCVD); or
molecular beam epitaxy (MBE).

Claim 39. (Previously Presented) The method of claim 36, wherein the strained Si layer is comprised of a semiconductor comprising one of Si or $Si_{1-y}C_y$.

Claim 40. (Previously Presented) The method of claim 36, further comprising forming additional $Si_{1-x}Ge_x$ on the $Si_{1-x}Ge_x$ layer to form a thicker $Si_{1-x}Ge_x$ layer.

Claim 41. (Previously Presented) The method of claim 40, further comprising

forming a strained Si layer on the thicker $Si_{1-x}Ge_x$ layer.

Claim 42. (Previously Presented) The method of claim 31, wherein the semiconductor structure is one of a nFET and a pFET.

Claim 43. (Previously Presented) The method of claim 31, wherein the plurality of channels include at least a first channel and a second channel and wherein the void is formed underneath the $Si_{1-x}Ge_x$ layer extending from at least the first channel to the second channel.

Claim 44. (Previously Presented) The method of claim 31, wherein the removing the top layer of the multi-layer substrate underneath the $Si_{1-x}Ge_x$ layer to form a void defined by an undercut border in the multi-layer substrate includes one of:

etching underneath the $Si_{1-x}Ge_x$ layer;

performing timed etching underneath the $Si_{1-x}Ge_x$ layer;

performing timed etching underneath the $Si_{1-x}Ge_x$ layer using an etchant that exhibits a higher etch rate for the multi-layer substrate than for $Si_{1-x}Ge_x$; and

performing timed etching underneath the $Si_{1-x}Ge_x$ layer using an etchant from a group consisting of ammonia, tetramethyl ammonium hydroxide, nitric acid and hydrofluoric acid.

Claim 45. (Previously Presented) The method of claim 31, wherein the $Si_{1-x}Ge_x$ layer has a bottom surface and a top surface, and the bottom surface is more resistant to etching than the top surface.

Claim 46. (Previously Presented) The method of claim 45, wherein the $Si_{1-x}Ge_x$ layer has a higher concentration of Ge at the bottom surface than at the top surface.

Claim 47. (Previously Presented) The method of claim 31, further comprising thermal annealing the $Si_{1-x}Ge_x$ layer after the filling of the channels and the void with the dielectric material.

Claim 48. (Previously Presented) The method of claim 31, further comprising planarization after the filling of the channels and the void with the dielectric material.

Claim 49. (New) A method of fabricating a semiconductor structure, comprising:

forming a $Si_{1-x}Ge_x$ layer on a substrate;

forming a plurality of channels in the $Si_{1-x}Ge_x$ layer and the substrate; and

after forming the plurality of channels, removing a layer of the multi-layer substrate underneath the $Si_{1-x}Ge_x$ layer to form a void defined by an undercut border in the substrate.

Claim 50. (New) The method of claim 49, further comprising filling the channels and the void with a material.

Claim 51. (New) The method of claim 49, wherein the forming of the plurality of channels in the $Si_{1-x}Ge_x$ layer is in a top layer of the substrate which is multi-layered.

Claim 52. (New) The method of claim 49, wherein:

the substrate includes a first silicon layer, a second insulator layer and a third substrate layer;

the plurality of channels include at least a first channel and a second channel extending through the $Si_{1-x}Ge_x$ layer to the bottom of the first silicon layer of the substrate; and

the void is formed in the first silicon layer of the substrate underneath the $Si_{1-x}Ge_x$ layer extending from at least the first channel to the second channel.

Claim 53. (New) The method of claim 49, wherein the step of removing a portion of the substrate underneath the $Si_{1-x}Ge_x$ layer includes one of:

etching the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer;

performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer;

performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer using an etchant that exhibits a higher etch rate for the substrate than for $Si_{1-x}Ge_x$; and

performing timed etching of the portion of the substrate underneath the $Si_{1-x}Ge_x$ layer using an etchant from one of ammonia, tetramethyl ammonium hydroxide, nitric acid and hydrofluoric acid.

Claim 54. (New) The method of claim 53, wherein the $Si_{1-x}Ge_x$ layer has a bottom surface and a top surface, and the bottom surface is more resistant to etching than the top surface and the $Si_{1-x}Ge_x$ layer has a higher concentration of Ge at the bottom surface than at the top surface.

Claim 55. (New) A method, comprising:

forming a $Si_{1-x}Ge_x$ layer on a multi-layered substrate;

forming a plurality of channels in the $Si_{1-x}Ge_x$ layer and the substrate;

after forming the plurality of channels, removing a top layer of the multi-layer substrate underneath the $Si_{1-x}Ge_x$ layer to form a void defined by an undercut border in the multi-layer substrate;

removing a portion of the multi-layered substrate underneath the $Si_{1-x}Ge_x$ layer to form a void; and

producing a relaxed portion of the $Si_{1-x}Ge_x$ layer above the void.

Claim 56. (New) The method of claim 55, wherein the void is formed in a first silicon layer of the multi-layered substrate underneath the $Si_{1-x}Ge_x$ layer extending from between at least two of the plurality of channels.